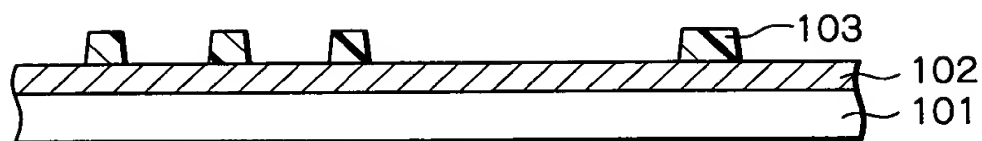


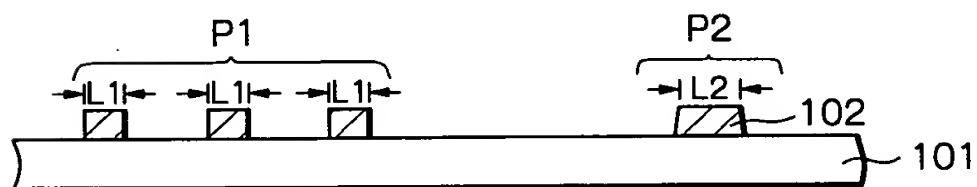
*Fig. 1A* PRIOR ART



*Fig. 1B* PRIOR ART

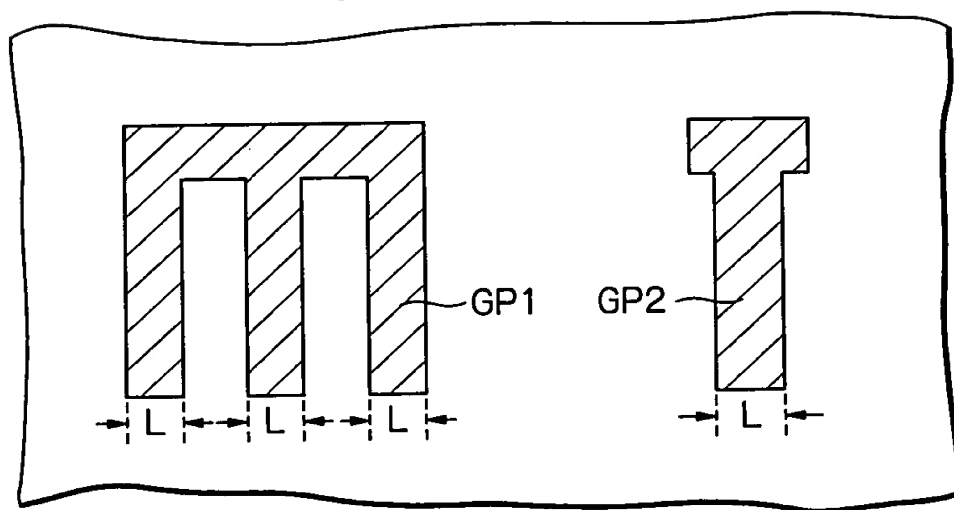


*Fig. 1C* PRIOR ART



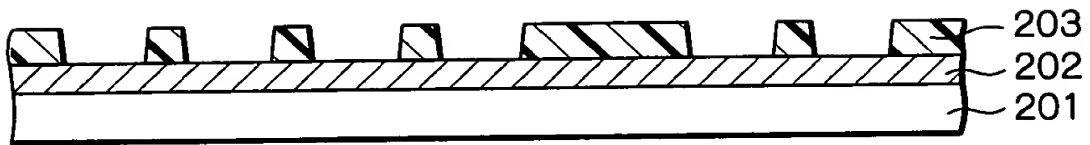
0973506-1400  
002121-5005260

*Fig. 2* PRIOR ART

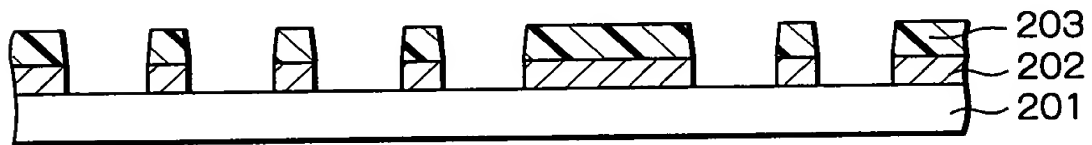


00735005-121300

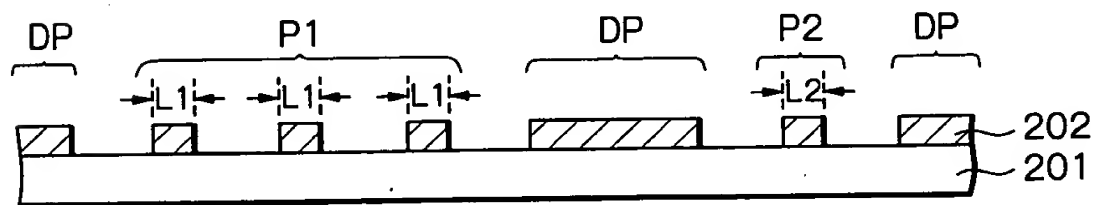
*Fig. 3A* PRIOR ART



*Fig. 3B* PRIOR ART

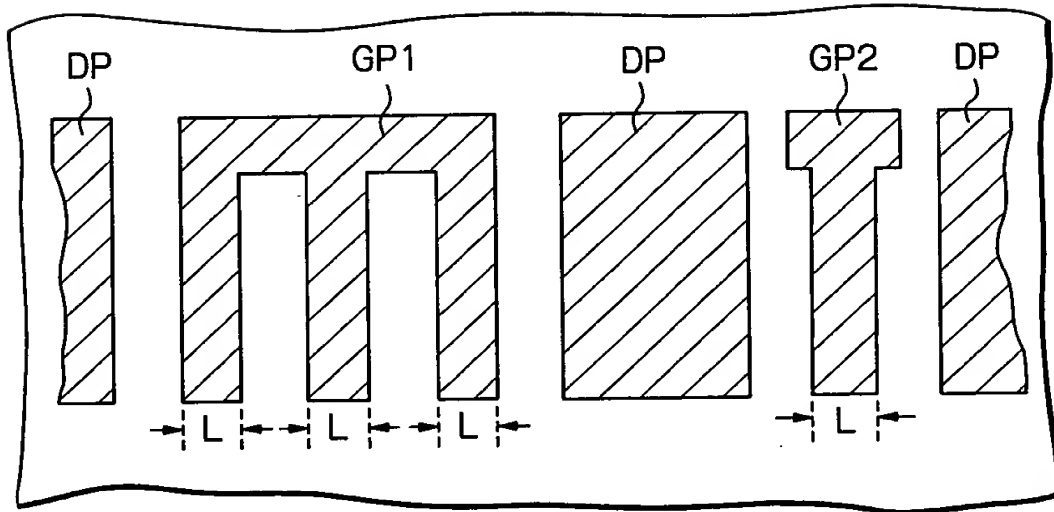


*Fig. 3C* PRIOR ART



002121-5005E260

*Fig. 4* PRIOR ART



0025005400

Fig. 5A

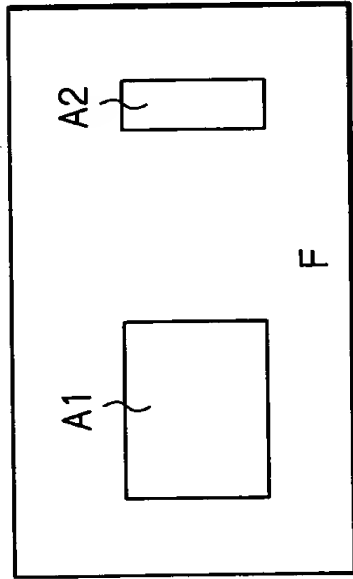


Fig. 5B

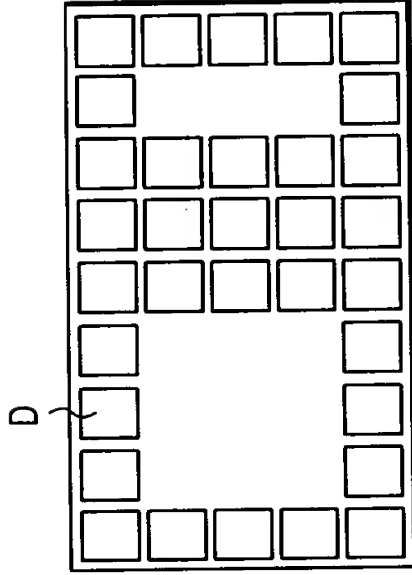


Fig. 5C

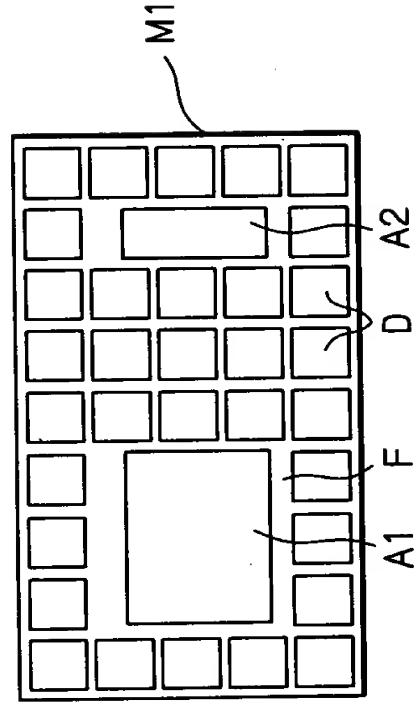


Fig. 6A

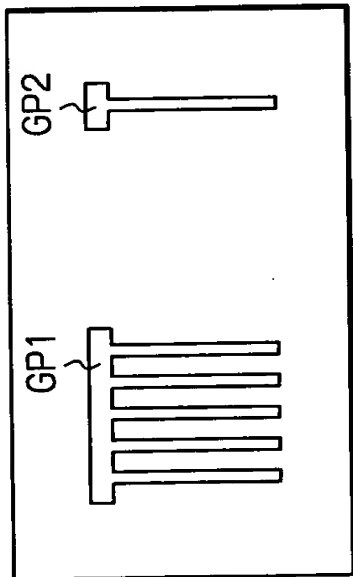


Fig. 6B

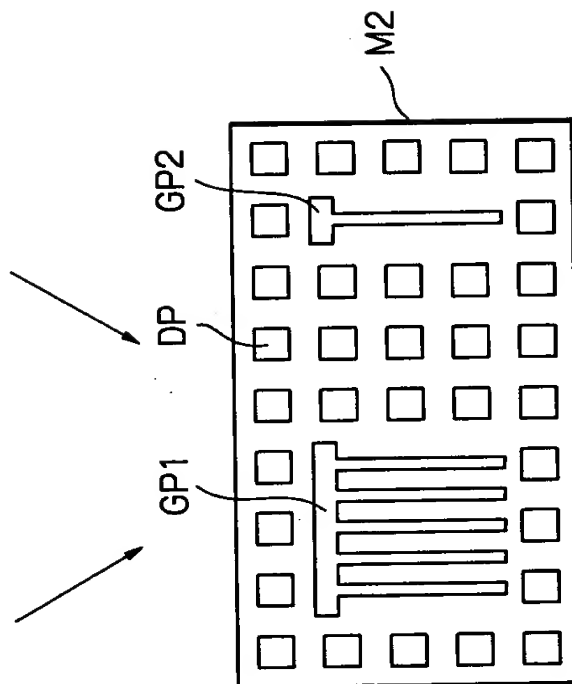
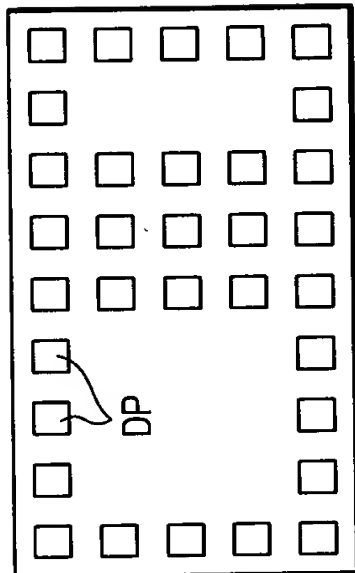
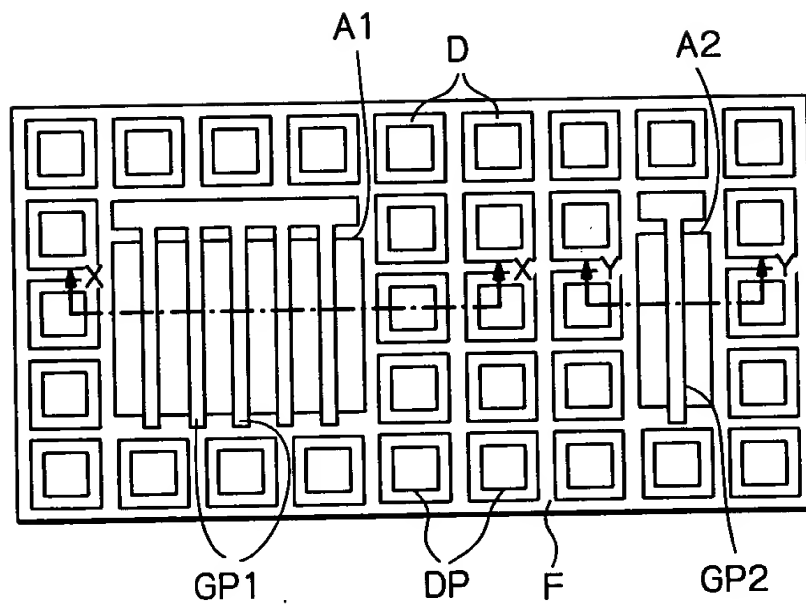


Fig. 6C

Fig. 7



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Fig. 8A

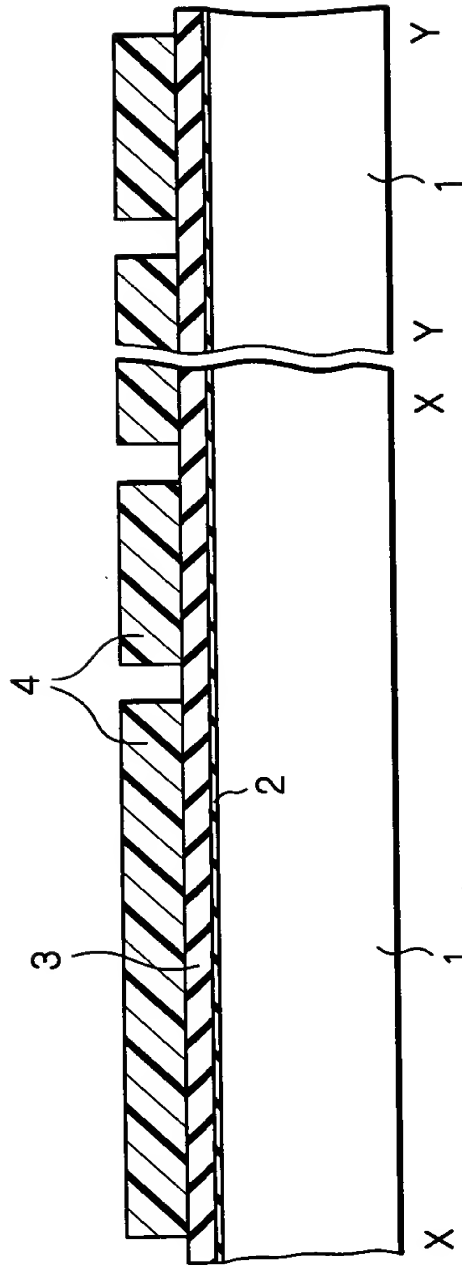


Fig. 8B

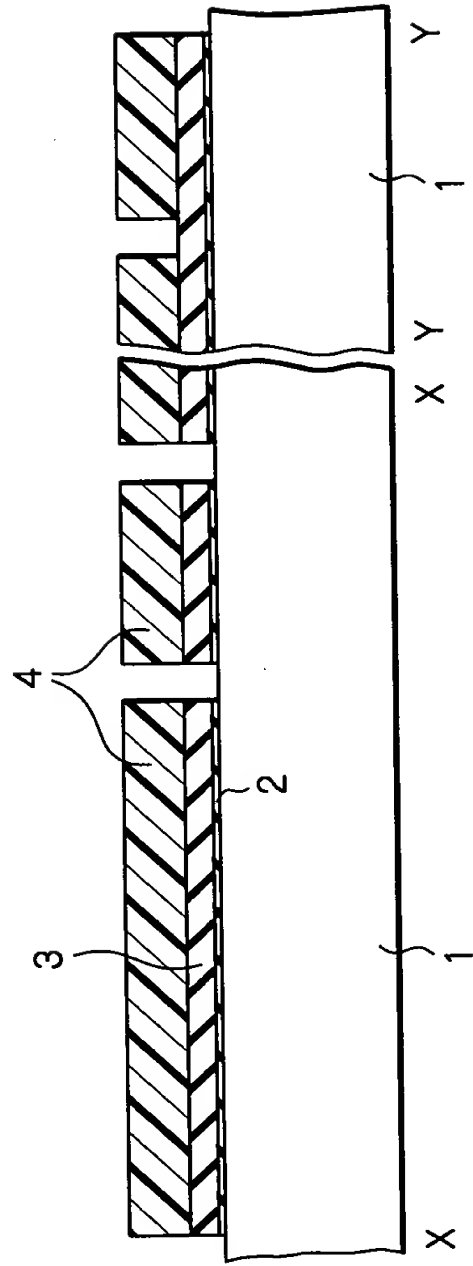






Fig. 8E

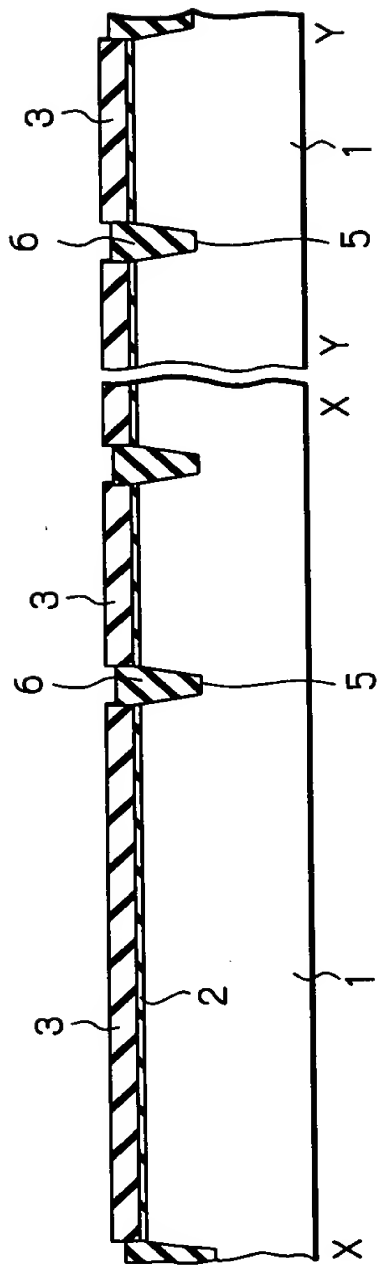
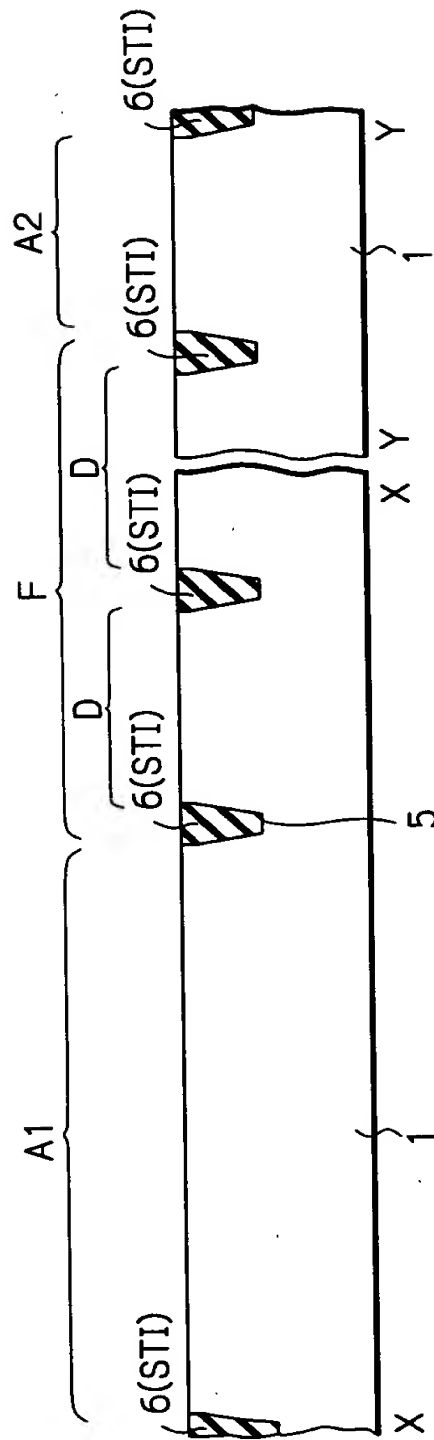
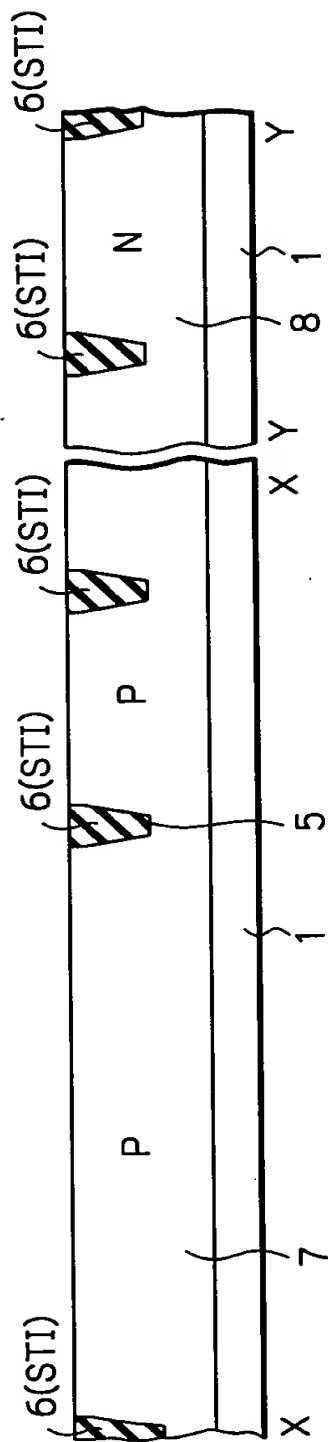


Fig. 8F



**Fig. 8G**



**Fig. 8H**

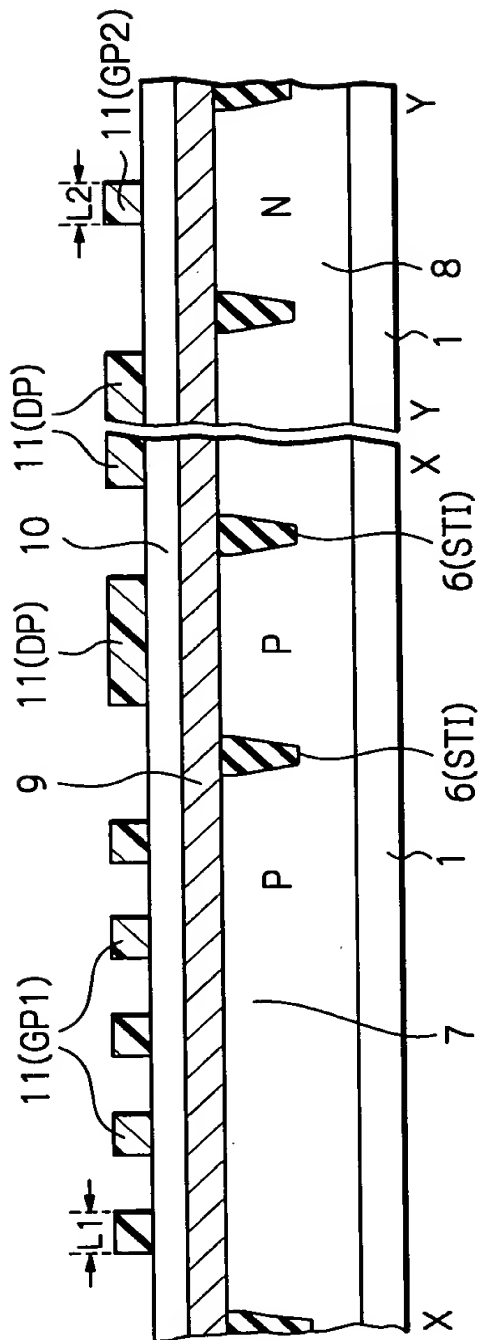


Fig. 8I

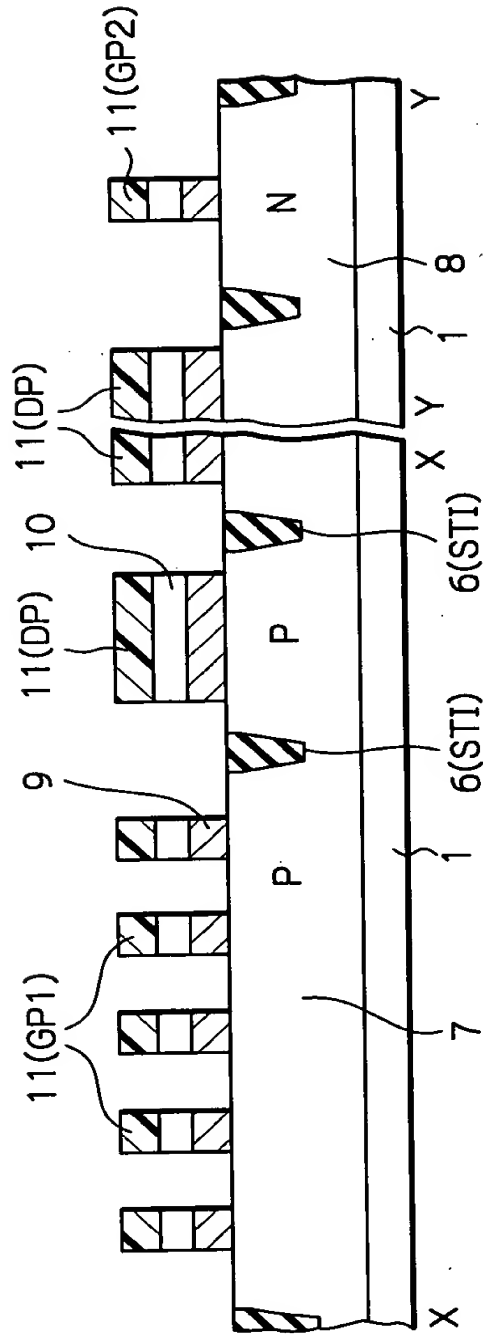


Fig. 8J

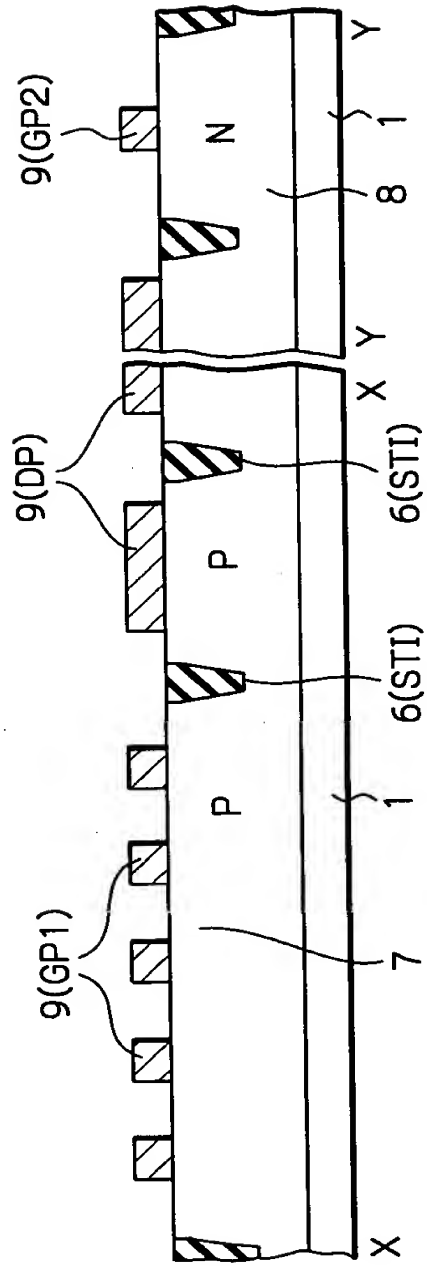


Fig. 8K

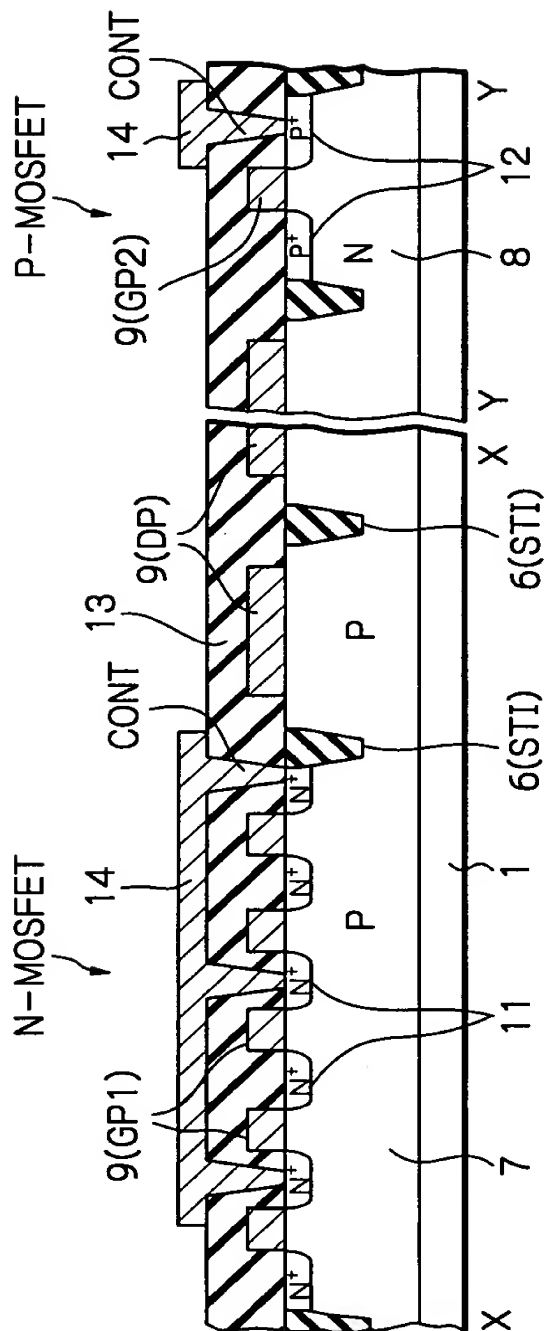
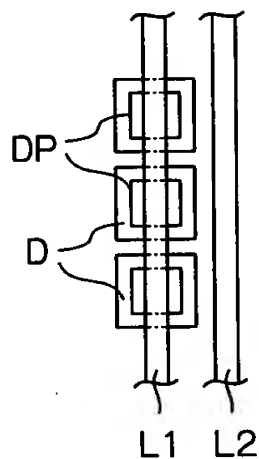




Figure 1 is a schematic diagram of a semiconductor device layout. It shows a grid of square patterns. Two large rectangular regions are labeled A1 and A2. Within A1, there are four vertical bars labeled GP1. Within A2, there are four vertical bars labeled GP2. A small square pattern is labeled F. A larger square pattern is labeled D. A small square pattern is labeled DP. A coordinate system is shown in the top right corner with X and Y axes.

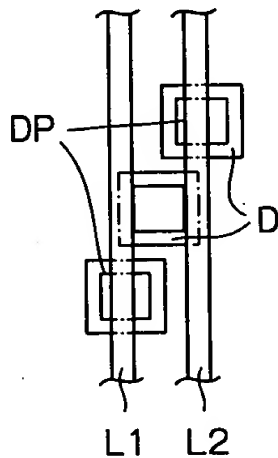
*Fig. 11A*

FIRST EMBODIMENT



*Fig. 11B*

SECOND EMBODIMENT



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